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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,307	04/02/2001	Kouichi Takagi	01190/LH	9372

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,307	TAKAGI ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

2. Claims 16, 21, and 26 are objected to because of the following informalities: missing the conjunction "and" before the final element of each claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Shiun et al., U.S. Patent 4348762, hereinafter referred to as Shiun.

4. As per claim 1, Shiun taught a clock generating circuit comprising of:

- a clock producing section to produce plural clocks differing in phase [FIG. 1, item 4; column 2, lines 9-11]; and
- a selecting section to select and output a first clock from the plural clocks and to switch from the first clock to a second clock with a different phase during a period the first clock is being outputted [column 2, lines 21-34].

5. As per claim 2, Shiun taught a switching control section to output a selection signal to indicate which clock is to be selected [column 2, lines 16-17].

6. As per claim 3, Shiun taught the switching control section to judge whether or not the first clock is switched to the second clock [column 2, lines 22-31].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7-8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiun as applied to claim 1 above.

9. As per claim 7, it would have been obvious for an ordinary artisan to integrate the clock generating device [FIG. 2].[1]

10. As per claim 8, it would have been obvious for an ordinary artisan to structure the clock generating device as digital.

11. As per claim 14, it would have been obvious for an ordinary artisan to incorporate the clock generating device on a base board.

12. Claims 4-6 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiun in view of Ashikaga, U.S. Patent 6215513.

13. Shiun taught a clock generating circuit producing a plurality of clocks with different phases selectable by a switch control section.

14. However, Shiun did not expressly disclose a method to control the period of switching between the plurality of different clock phases.

15. Ashikaga taught a clock generating device comprising of a plurality of clocks with different phases used in an imaging device.

16. As per claim 4, Ashikaga taught a switching control section to produce the selection signal based on predetermined output clock information [FIG. 2; column 6, lines 22-25].

17. As per claim 5, Ashikaga taught a memory section to store the output clock information [FIG. 2, item LATCH].

18. As per claim 6, Ashikaga taught a calculating section to calculate the output clock information [column 6, lines 39-45].

19. As per claim 9, Ashikaga taught an entire control section to control the clock generating device [FIG. 8, item 5].

20. As per claim 10, Ashikaga taught a control counter section to produce region information to indicate a region to be switched to the second clock based on region data received by the entire control section and the switching control section produces the selection signal based on the region information [column 6, line 39 to column 7, line 19].

21. As per claim 11, Ashikaga taught a clock producing section comprising a reference clock generating section and a delay chain section to produce plural different delay clocks based on the reference clock [FIG. 3].

22. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to better control the output of a poly-phase generating clock circuit when the data to be read comprises of regions requiring different clock phases [see Ashikaga: column 1, lines 19-31].

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[1] In re Larson, 340 F.2d 965, 967, 144 USPQ 347, 349 (CCPA 1965); In re Wolfe, 251, F.2d 854, 855, 116 USPQ

23. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Shiun and Ashikaga to provide a clock generating device capable of switching among different phases within a predetermined region.

24. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ashikaga as applied to claim 11 above, and further in view of Guo, U.S. Patent 5451894.

25. Ashikaga taught a clock generating device capable of switching among different clocks within a predetermined region by finding an optimum clock in synch with a trigger time [column 8, lines 34-41].

26. However, Ashikaga did not expressly disclose the method to determine the synchronized clock among the plurality of delay stages.

27. Guo taught a digital clock phase shifter comprising of a plurality of delay stages. The device is operable to detect the particular delay stage in synch with a reference clock [column 3, lines 16-23].[2]

28. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to determine synchronization information for data recovery or other similar tasks employing a system with a plurality of delay stages [see Guo: column 1, lines 47-58].

29. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Guo and Ashikaga to provide a clock generating device capable of switching among different phases within a predetermined region utilizing synchronization information.

443, 444 (CCPA 1958)

[2] Each delay stage corresponds to a different clock phase. With a constant delay for each stage, locating one particular stage in synch with the reference clock would enable the determination of the number of possible in-synch stages in a system with known finite number of delay stages.

30. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ashikaga, U.S. Patent 6215513, in view of Guo, U.S. Patent 5451894.

31. Ashikaga taught a clock generating device comprising of:

- a reference clock generator [FIG. 1, item 7];
- a delay chain section to produce plural delay clocks based on the reference clock [FIG. 3];
- an entire control section to control the clock generating device [FIG. 8, item 5];
- a control counter section to produce region information to indicate a region to be switched to the second clock based on region data [column 6, line 39 to column 7, line 19];
- a switching control section to produces the selection signal [FIG. 2; column 6, lines 22-25]; and
- a selecting section to select and output the first clock and to switch from the first clock to a second clock within a predetermined time period based on the selection signal outputted from the switching control section [FIG. 2, item 9; column 6, lines 14-21, lines 60-63].

32. However, Ashikaga did not expressly disclose the method to determine the synchronized clock among the plurality of delay stages.

33. Guo taught a digital clock phase shifter comprising of a plurality of delay stages. The device is operable to detect the particular delay stage in synch with a reference clock [column 3, lines 16-23].[3]

34. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to determine synchronization information for data recovery or other similar tasks employing a system with a plurality of delay stages [see Guo: column 1, lines 47-58].

35. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Guo and Ashikaga to provide a clock generating device capable of switching among different phases within a predetermined region utilizing synchronization information.

36. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiun as applied to claim1 above, and further in view of Ashikaga, U.S. Patent 6215513.

37. Shiun taught a clock generating circuit producing a plurality of clocks with different phases selectable by a switch control section.

38. However, Shiun did not expressly disclose a method to control the period of switching between the plurality of different clock phases based on a predetermined region.

39. Ashikaga taught an imaging device comprising of

- a writing device to write an image based on the clock outputted from the select section [FIG. 5, LED PRINT HEAD]; and

[3] Each delay stage corresponds to a different clock phase. With a constant delay for each stage, locating one particular stage in synch with the reference clock would enable the determination of the number of possible in-synch stages in a system with known finite number of delay stages.

- the writing device writes an image to be located in a predetermined region based on the second clock and an image to be located outside of the predetermined region based on the first clock [column 11, lines 17-35].

40. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to better control the output of a poly-phase generating clock circuit when the data to be read/written comprises of regions requiring different clock phases [see Ashikaga: column 1, lines 19-31].

41. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Shiun and Ashikaga to provide a clock generating device capable of switching among different phases within a predetermined region.

42. Claims 16-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashikaga and Guo as applied to claim 13 above, and further in view of Stinson et al., U.S. Patent 6127858, hereinafter referred to as Stinson.

43. As per claims 16, 17, 22, and 27, Ashikaga and Guo combined taught a clock generating device comprising of:

- a delay chain section to produce plural delay clocks based on the reference clock [see Ashikaga: FIG. 3];
- a synchronous detecting section to derive synchronous information corresponding to a delay stage number of one cycle from the selected plural delay clocks [see Guo: column 3, lines 16-23; column 4, lines 17-24; column 5, lines 16-35];[4] and

[4] Each delay stage corresponds to a different clock phase. With a constant delay for each stage, locating one particular stage in synch with the reference clock would enable the determination of the number of possible in-synch stages in a system with known finite number of delay stages.

- a select section to select a synchronous clock with the reference clock from the delay chain section [see Guo: column 3, lines 20-27; column 5, lines 25-27].

44. However, Ashikaga and Guo did not expressly disclose the method to disperse time intervals between the two clock signals.

45. Stinson taught an invention to vary a frequency of an input clock with a plurality of delay stages by alternating between two delay stages to create an optional clock [FIG. 5; column 2, line 46 to column 3, line 4].

46. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to vary the frequency of a clock generating device that can be used to test a myriad of electronic components [see Stinson: column 1, lines 12-19, lines 46-67].

47. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Stinson, Guo, and Ashikaga to provide a clock generating device capable of switching among different phases to produce a clock with varied frequency.

48. As per claims 18, 23, and 28, it would have been obvious for an ordinary artisan to integrate the clock generating device [FIG. 2].[5]

49. As per claims 19, 24, and 29, it would have been obvious for an ordinary artisan to structure the clock generating device as digital.

50. As per claims 20, 25, and 30, Ashikaga taught an imaging device utilizing clock generating device [FIG. 5; FIG. 8].

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[5] In re Larson, 340 F.2d 965, 967, 144 USPQ 347, 349 (CCPA 1965); In re Wolfe, 251, F.2d 854, 855, 116 USPQ 443, 444 (CCPA 1958)

51. As per claim 21, Stinson taught a switching control section to disperse time intervals between clock signals by conducting alternately between two clocks in a way as to subtract an optional time [FIG. 7, item 702; column 2, lines 55-58].

52. As per claim 26, Stinson taught a switching control section to disperse time intervals between clock signals by selecting and conducting alternately between two clocks in a way as to add and subtract an optional time [FIG. 5; column 2, lines 55-58, lines 63-66].

53. As per claim 31, Ashikaga taught a predetermined time period to perform clock switching [column 6, line 39 to column 7, line 19; column 8, lines 34-41].

Conclusion

54. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Honbo et al., U.S. Patent 5677725, disclosed an imaging device utilizing two delay clocks to output a desired clock.

b. Danger, U.S. Patent 5719515, disclosed a digital delay chain.

c. Backes, U.S. Patent 4618788, disclosed an integrated, digital delay circuit.

d. Grimes et al., U.S. Patent 4672299, disclosed a phase control circuit.

e. Shin, U.S. Patent 6212249, disclosed a method to synchronize a reference clock with the data being read.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (703) 305-8580. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
March 2, 2004

THOMAS LEE
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